Amendments to the Specification:

Please replace the paragraph beginning a line 1 of page 9 with the following paragraph.

Figure 7 further illustrates how the movement of the ~~Vsync~~ Vertical synchronization signal controls the position of the image display up or down on the LCD panel. Fig. 7 shows the blanked out areas 701, 703 of the display data as well as the even frames of displayable data 702, 704. There are three cases illustrated in figure 7. Case 1 shows the ~~Vsync~~ Vertical synchronization pulse lined up with the transition from blank data to Even frame displayable data 710. The corresponding LCD image display showing the displayable image starting at the top of the LCD 720. Case 2 shows the ~~Vsync~~ Vertical synchronization pulse occurring in the middle of the blank data 730. The corresponding LCD image display showing the displayable image centered in the middle of the LCD 740. Case 3 shows the ~~Vsync~~ Vertical synchronization pulse lined up with the transition from even displayable data to ~~bland~~ blank data 750. The corresponding LCD image display showing the displayable image skewed toward the bottom of the LCD 760.

Please replace the paragraph beginning a line 13 of page 9 with the following paragraph.

Figure 6 also illustrates that the frequency of the ~~Vsync~~ Vertical synchronization of the LCD panel is one half of the frequency of the ~~Vsync~~ Vertical synchronization of the source. Also, the ~~frequencey~~ frequency of the horizontal synchronization signal Hsync of

the LCD panel 650 equals the Hsync of the source 620. Therefore, the ~~Vsync~~ Vertical synchronization frequency requirements are equal to or less than those of the source.

Please add the following new figure listing after line 20 on page 6.

FIG. 8 shows a circuit block diagram of the main embodiment of this invention.

Please add the following new paragraph after line 17 on page 9.

Figure 8 shows a block diagram of the circuitry of the main embodiment of this invention. The image frame buffer 810 used by the digital signal processing, DSP, circuitry is shown. No additional frame buffers are required. Similarly, the line buffers 830 used by the DSP circuitry is shown. No additional line buffers are required. Figure 8 also shows a direct connection 860 between the output of the image frame buffer 810 and the line buffer 830. It also shows a direct connection 840 between the line buffer 830 and the LCD panel driver 850 which drives the LCD panel 820. Figure 8 also shows a program retention device 870, which is a networked 875-computer device. The program instructions are stored in a program memory 880 shown. These program instructions 880 are used to eliminate the need for a frame buffer. The computer 870 moves the no scaling image and also simulates a model of an LCD panel without scaling. Figure 8 also shows a frequency divider 890, which is used to divide the frequency of the Vertical synchronization of the source image buffer by two. This half frequency is used to drive the LCD panel. Figure 8 also shows logic circuitry 895, which is used to blank the display

during the odd frame time domain. This is known as skipping an LCD Vertical synchronization at the end of the display within the even image lines. This logic circuitry 895 utilizes a shift register to shift the position of the Vertical synchronization in the time domain for the LCD panel.